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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/764,165

01/23/2004

Ken Gary Pomaranski

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08/08/2006

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EXAMINER

CHU, GABRIEL L

ART UNIT

PAPER NUMBER

2114

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/764,165	Applicant(s) POMARANSKI ET AL.	
	Examiner Gabriel L. Chu	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 8-10 and 18-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,6,7,11,12 and 14 is/are rejected.
- 7) ☒ Claim(s) 3-5,13 and 15-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20050523 20040123</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 23 May 2005 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. Specifically, EP 1416695 is in German.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-7, 11-17, drawn to an invention directed to status signal generation, classified in class 714, subclass 48.

II. Claims 8-10, 18-20, drawn to an invention directed to status propagation, classified in class 714, subclass 57.

The inventions are distinct, each from the other because of the following reasons: In the instant case the different inventions perform one of status generation and status propagation. These inventions have different operations, functionality, and effects.

These inventions are described separately in the specification. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with James Okamoto on 3 August 2006 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-7, 11-17. Affirmation of this election must be made by applicant in replying to this Office action. Claims 8-10, 18-20 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 6, 7, 11, 12 rejected under 35 U.S.C. 102(b) as being anticipated by US 2002/0027881 to Castellano et al.** Referring to claim 1, 11, Castellano discloses receiving a first status signal from a computational node (Figure 1, 53.);

generating a default status signal (Figure 1, 72, but also the signals of 53 are all generated automatically in the determination of the quality indicator signal.);

and using the first status signal and the default status signal to generate a second status signal (From paragraph 35, "The quality indicator logic receives a clocking signal 72 from the local network chip's timing circuit. The clocking signal is used to provide timing information for the quality indicator logic module to generate a plurality of link quality indicator signals with various timing characteristics.").

6. Referring to claim 6, Castellano discloses receiving a first degraded status signal from the computational node; generating a default degraded status signal (Figure 1, the

signals of 53 are all generated automatically in the determination of the quality indicator signal.);

and using the first degraded status signal and the default degraded status signal to generate a second degraded status signal (From paragraphs 39, 40, "If the local network chip detects a false carrier sense signal or a receive coding error signal, the link quality indicator signal is driven high then low at a low frequency 92. This creates a first periodic link quality indicator signal indicating that the network link is marginally operational because there are framing or receive coding errors. If the local network chip detects that the MSE is greater than the SNR threshold value, then the link quality indicator signal is driven high then low at a high frequency 92. This creates a second periodic link quality indicator signal indicating that the network link is marginally operational because the MSE is higher than the SNR threshold value.").

7. Referring to claim 7, Castellano discloses the degraded status signals include multiple levels of degradation (From paragraphs 39, 40, "If the local network chip detects a false carrier sense signal or a receive coding error signal, the link quality indicator signal is driven high then low at a low frequency 92. This creates a first periodic link quality indicator signal indicating that the network link is marginally operational because there are framing or receive coding errors. If the local network chip detects that the MSE is greater than the SNR threshold value, then the link quality indicator signal is driven high then low at a high frequency 92. This creates a second periodic link quality indicator signal indicating that the network link is marginally operational because the MSE is higher than the SNR threshold value.").

8. Referring to claim 12, Castellano discloses the output signal generator includes a voltage-level pulling element operative on the first status signal (Figure 2, 202. Also, wherein the "first status signal" is a voltage, it is either pulled up or down to indicate a value.).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claims 2, 14 rejected under 35 U.S.C. 103(a) as being unpatentable over US 20020027881 to Castellano et al. as applied to claim 1, 11 above, in view of US 6862695 to Lin.** Referring to claim 2, 14, Castellano discloses if the first status signal indicates an up state, then the second status signal comprises an assigned first signal indicative of the up state, and wherein if the first status signal indicates a down state, then the second status signal comprises an assigned second signal indicative of the down state (From paragraph 37 and 38, "If the quality indicator logic module determines that the network link is functioning normally, the link quality indicator signal is driven low and remains low as long as the network link is functioning normally 86. This creates a first aperiodic link quality indicator signal indicating that the network link is fully operational. If the local network chip is unable to establish and maintain a network channel with the remote network device, then the link quality indicator signal is driven

high 88 and it remains in that state until the local network chip can reestablish the network channel. This creates a second aperiodic link quality indicator signal indicating that the network link is not operational at all.”). Castellano further discloses periodic signals indicative of state (From paragraphs 39, 40, “If the local network chip detects a false carrier sense signal or a receive coding error signal, the link quality indicator signal is driven high then low at a low frequency 92. This creates a first periodic link quality indicator signal indicating that the network link is marginally operational because there are framing or receive coding errors. If the local network chip detects that the MSE is greater than the SNR threshold value, then the link quality indicator signal is driven high then low at a high frequency 92. This creates a second periodic link quality indicator signal indicating that the network link is marginally operational because the MSE is higher than the SNR threshold value.”).

Although Castellano does not specifically disclose that the assigned first and second status signals indicative of up/down states may have been assigned as the periodic signals, Castellano in the disclosure has disclosed 4 states each representable by a choice of LED states. Assigning the periodic states specifically to up and down states would have been a decision made by the designer of such a system. Evidence of this is shown by line 41 of column 2 of Lin, “The BIOS program tests a first hardware device by identifying the type and ID of the first hardware device. If the first hardware device is tested to be failed, a single luminescent display is provided to blink ON and OFF at a first frequency. Hereinafter, the BIOS program tests a second hardware device which is assigned to the BIOS memory according to the preferred embodiment of

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the present invention, by checking the error detection value contained at the predetermined memory location of the BIOS memory to detect whether the BIOS program contains error. If the BIOS program is detected to contain error, the single luminescent display will blink ON and OFF at a second frequency which is different from the first frequency. Eventually, the BIOS program tests a third hardware device by identifying the type and ID of the third hardware device. If the third hardware device is tested to be failed, the single luminescent display will blink ON and OFF at a third frequency which is different from the first frequency and the second frequency."

Allowable Subject Matter

11. Claims 3-5, 13, 15-17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Referring to claim 3-5, 15-17 the prior art does not teach or fairly suggest in light of the parent claims, if the first status signal indicates neither up nor down states, then the second status signal defaults to the second periodic signal.

12. Referring to claim 13, the prior art does not teach or fairly suggest in light of the parent claim, the output signal generator includes an exclusive-or circuit operative on the first status signal and the default status signal.

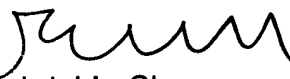
Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Gabriel L. Chu
Examiner
Art Unit 2114